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A Sigma-Delta Resistance to Digital Converter Suitable for Differential Resistive Sensors

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Abstract *– This paper presents a novel resistance-to-digital converter (RDC) suitable for differential resistive sensors. The proposed RDC provides a digital output linearly proportional to the parameter being sensed by a differential resistive sensor not only for differential resistive sensors possessing linear characteristic but also for sensors possessing inverse characteristic. The proposed RDC is based on the sigma-delta type analog-to-digital converter (Σ–Δ ADC) principle and hence possesses all the advantages and limitations of a Σ–Δ ADC. Experimental results on a prototype built and tested gave a worst case error < 0.15 %, establishing the efficacy of the proffered RDC.*

Keywords *– Sigma-delta converter, resistance-to-digital converter, differential resistive sensor.*

I. INTRODUCTION

A transducer is necessary to interface real world variables such as displacement, pressure and temperature to an electronic instrumentation system. A typical transducer consists of a sensor operated upon by a signal conditioning circuit that provides an analog voltage or current output. Present day instrumentation systems are of the digital kind as digital systems offer increased processing power and excellent user interface compared to their analog counterparts. An analog-to-digital converter (ADC) is required to interface a transducer with an analog output to a digital instrumentation system [1]. It would be advantageous if the signal conditioning part of a transducer provides a direct digital output so that the transducer can be interfaced to a digital instrumentation system without the need for an intervening ADC. Such direct capacitance-to-digital converters (CDC) based on relaxation oscillator principle [2] and sigma-delta ADC principle [3] have been reported. Techniques that provide resistance-to-digital conversion using an RC oscillator and timer-counter [4], resistance-to-frequency [5] and resistance-to-time [6] conversions are reported but these methods are suitable only for single element resistive sensors. Methods suitable for differential resistive sensors based on integrating type ADC have been reported [7]-[9].

We now propose a novel direct resistance to digital converter (RDC) suitable for differential resistive sensors. The proposed scheme is based on the popular sigma-delta ADC principle and accepts differential resistive sensors possessing either linear or inverse characteristics and provides a linear digital output proportional to the measurand being sensed by the differential resistive sensor.

II. SIGMA-DELTA RESISTANCE TO DIGITAL CONVERTER

A functional block diagram of the proposed Σ-Δ resistance-to-digital converter is shown in Fig. 1. As in a typical Σ-Δ ADC [10], the proposed scheme has a Δ modulator followed by an over-sampler and a digital filter. In Fig. 1, $+V_R$ and $-V_R$ are dc reference voltages of equal

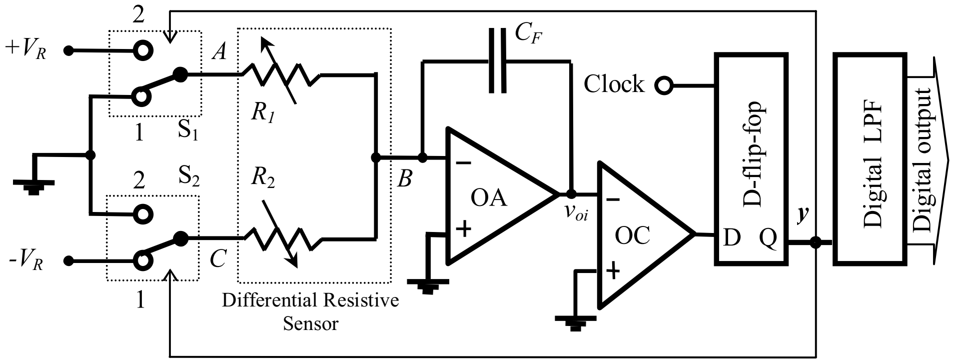

Fig. 1 Proposed sigma-delta resistance to digital converter

magnitude but of opposite polarities. Opamp OA with capacitor C_F in its feedback path and resistors R_1 and R_2 of a differential resistive sensor in combination with two single-pole-double-throw (SPDT) analog switches S_1 and S_2 serving as input, form an integrator. The integrator output v_{oi} is fed to a comparator OC whose output is "low" if $v_{oi} \geq 0$ and "high" otherwise. Output of OC is given to the input of a D-flip-flop whose output $\boldsymbol{y}$, controls switches S_1 and S_2. Switches S_1 and S_2 are set at position 1 if $\boldsymbol{y} = 1$ and set at position 2 whenever $y = 0$. The D-flip-flop output $\boldsymbol{y}$, updated (say at the leading edge) by a high frequency clock of time period Tc, is also fed as input to a digital low-pass filter (LPF) based circuitry which extracts and provides the final output as $\left(1-2\boldsymbol{y}|_{avg}\right)$, where $\boldsymbol{y}|_{avg}$ is the average value of the LPF input bit stream $\boldsymbol{y}$.

To start with let $v_{oi} < 0$ and $\boldsymbol{y} = 1$, hence switches S_1 and S_2 are set at position 1. For this condition, R_1 is connected to ground through switch S_1, R_2 is tied to $-V_R$ through switch S_2. Hence v_{oi} ramps-up with a slope of (V_R/R_2C_F) till v_{oi} becomes positive. Once v_{oi} is positive, comparator output becomes low. The D-flip-flop output gets updated at the very next (leading edge of the) clock and hence the output $\boldsymbol{y}$ toggles ($\boldsymbol{y}$ = 0). When $\boldsymbol{y}$ = 0, switches S_1 and S_2 are set to position 2, grounding resistance R_2 and connecting R_1 to $+V_R$. Now the current V_R/R_1 charges C_F, consequently, v_{oi} ramps down with a slope V_R/R_1C_F till v_{oi} turns negative, forcing the output of the comparator to go high. The D-flip-flop output gets updated on the next clock and hence $\boldsymbol{y} = 1$, bringing the status of the circuit to its assumed initial condition and hence the entire cycle repeats continuously. When $\boldsymbol{y}$ = 1, change in integrator voltage for each clock period, $\Delta v_{oi(1)} = V_R T_C / R_2 C_F$. Similarly, for $\boldsymbol{y}$ = 0, the change in integrator voltage for each clock period is $\Delta v_{oi(0)} = -V_R T_C / R_1 C_F$. After a finite number of clock cycles, say N ($=T/T_C$) the integrator output is

$$v_{oi(N)} = \frac{V_R T_C}{R_2 C_F} N_{(1)} - \frac{V_R T_C}{R_1 C_F} N_{(0)} \quad . \tag{1}$$

Here $N = N_{(1)} + N_{(0)}$, $N_{(1)}$ is the number of clock cycles for which the output of D-flip-flop is 1 and $N_{(0)}$ is the number of clock cycles for which the output of D-flip-flop is 0. If N is sufficiently large then the value of $v_{oi(N)}$ has to be less than or equal to the maximum possible change in integrator voltage per clock cycle $v_{oi(\mathrm{m})}$, where

$$v_{oi(\mathrm{m})} = V_R T_C \big/ (R_1, R_2)_{\min} C_F \ . \tag{2}$$

Here $(R_1, R_2)_{\min}$ is the minimum among R_1 and R_2. Then

$$\frac{V_R T_C}{C_F}\left(\frac{N_{(1)}}{R_2} - \frac{N_{(0)}}{R_1}\right) \leq \frac{V_R T_C}{C_F}\frac{1}{(R_1, R_2)_{\min}} \ . \tag{3}$$

On further simplification we get:

$$\left(N_{(1)}R_1 - N_{(0)}R_2\right) \leq (R_1, R_2)_{\max} \tag{4}$$

where $(R_1, R_2)_{\max}$ is the maximum of R_1 and R_2. If the differential resistive sensor possesses linear characteristics then

$$R_1 = R_0(1 \pm kx) \ \text{ and } \ R_2 = R_0(1 \mp kx) , \tag{5}$$

where R_0 is the nominal value of the sensor resistances, x the quantity being sensed and k the transformation factor. Substituting the values of R_1 and R_2 from (5) in (4) results in

$$\left(R_0(1 \pm kx)N_{(1)} - R_0(1 \mp kx)N_{(0)}\right) \leq (R_1, R_2)_{\max} \ .$$

$$\Rightarrow \frac{R_0}{N}\left[(N_{(1)} - N_{(0)}) \pm kxN\right] \leq \frac{1}{N}(R_1, R_2)_{\max} \ .$$

For a very large value of N the value of $\frac{1}{N}(R_1, R_2)_{\max}$ becomes small and hence

$$kx = \left[\frac{N_{(0)} - N_{(1)}}{N}\right] = 1 - 2\left(\frac{N_{(1)}}{N}\right) = \left(1 - 2\boldsymbol{y}|_{avg}\right) . \tag{6}$$

Here, $\left(N_{(1)}/N\right)$ is the average value $\boldsymbol{y}|_{avg}$ of the bit-stream $\boldsymbol{y}$ over the period NT_C. As mentioned earlier, the digital low-pass filter based circuitry is designed to extract $\left(1-2\boldsymbol{y}|_{avg}\right)$ thus its output is kx. Hence for differential resistive sensors possessing linear characteristics as given in (5), the proposed technique provides a linear digital output proportional to the quantity being sensed. Very rarely differential resistive sensors possess inverse characteristics, wherein

$$R_1 = \frac{R_0}{(1 \mp kx)} \ \text{ and } \ R_2 = \frac{R_0}{(1 \pm kx)} . \tag{7}$$

It nicely turns out that substituting the values R_1 and R_2 from (7) in (4) also results in (6). Thus, the proposed method provides a linear digital output proportional to the measurand even if the differential resistive sensor follows an inverse relationship as given in (7). The experimental detail of a prototype RDC built and tested using off-the-shelf components is given next.

III. EXPERIMENTAL SET-UP AND RESULTS

A prototype Σ–Δ resistance to digital converter has been built and tested in a laboratory environment. Reference voltage $+V_R$ was generated using reference diode LM385 followed by a low offset opamp OP07 connected as a voltage follower. Then a unity gain inverter realised with another OP07 provided $-V_R$ from $+V_R$. Magnitudes of $-V_R$ and $+V_R$ were matched up to 5 digits. SPDT switches were realised with IC MAX4680 (possessing low ON resistance r_{ON} of

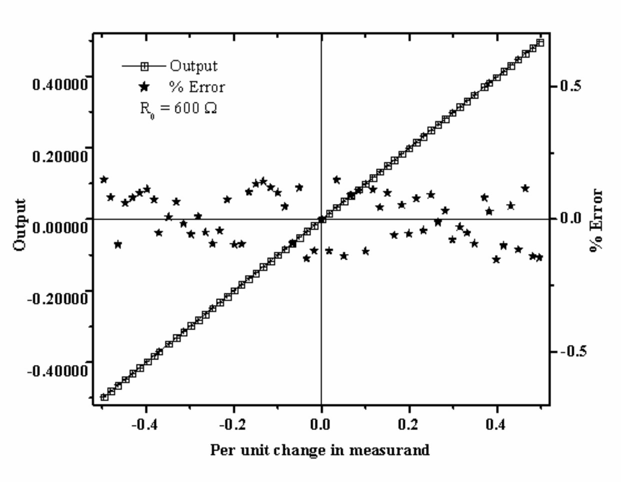

Fig. 2 Experimental results of the prototype Σ–Δ RDC

1.25 Ω). A third OP07 served as opamp OA. The value of the feedback capacitor is chosen as 0.1µF. An LM311 IC served as comparator OC and CD4013 was employed for the D-flip-flop. To extract $y|_{avg}$, IC AD1556 was employed. The AD1556 implements a Finite Impulse Response (FIR) linear phase equi-ripple low pass filter and decimator [11]. The modulator clock frequency for the AD1556 was chosen to be 20 kHz. A suitable program was written and burnt into a PIC16F877A microcontroller [12] to read the output $y|_{avg}$ from AD1556, compute and display $\left(1-2y|_{avg}\right)$ on a 5-digit seven segment display. The conversion time of the prototype Σ–Δ RDC developed is 40 ms. The prototype developed was tested with resistive sensors possessing linear as well as inverse characteristics. To test the performance of the prototype RDC, transducer resistances were simulated with two precision, decade resistance boxes from Otto Wolff, Germany, having a resolution of 1Ω and an accuracy of ±0.01%. The nominal value of the resistances is selected as 600 Ω and the two resistances were varied up to 300 Ω in steps of 10 Ω to simulate a *kx* variation in the range of ±0.5. The output characteristic along with error of the prototype is shown in Fig. 2. The worst case error was found to be less than ±0.15%.

IV. CONCLUSION

A sigma-delta type direct resistance-to-digital converter (RDC) apposite for differential resistive sensors has been developed. The developed RDC provides a linear digital output proportional to the change in the measurand being sensed, not only for sensors possessing linear characteristic, but also for sensors possessing inverse characteristic. In the developed RDC, the differential resistive sensor is an integral part of a first order 1-bit quantiser of a conventional Σ–Δ ADC. The quantiser is controlled appropriately so that the final digital output is made to be proportional to the measurand being sensed by the differential resistive sensor. The proposed RDC has all the advantages and limitations applicable to a Σ–Δ ADC. A prototype built and tested establishes the practicality of the proposed RDC. The worst-case error of the prototype was found to be less than ± 0.15 %. This type of RDC is best suited for MEMS type of applications.

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